WHAT IS CLAIMED IS:

1. A method of providing self-aligning features on a semiconductor device comprising the steps of:

providing a substrate with a dielectric layer that defines at least one line of metallization;

recessing the top surface of said at least one line of metallization below the top surface of said dielectric layer;

capping said at least one line of metallization with a barrier layer deposited over the top surface of said substrate, said barrier layer defining a top surface that follows the contours of the top surface of said at least one line of metallization and said dielectric;

depositing a layer of liner material over said barrier layer, said layer also following the contours of said at least one line of metallization and said dielectric;

planarizing said layer of liner material so as to remove high areas such that the low areas of said liner material remain; and

etching selected features in said dielectric layer of said substrate by using said remaining low areas of said liner material as a hard mask.

2. The method of claim 1 wherein said barrier layer is selected from silicon nitride and silicon carbide.

3. The method of claim 1 further comprising the step of depositing an ILD (intermediate layer dielectric) layer over said capping layer before depositing said layer of liner material.

4. The method of claim 1 wherein said layer of liner material is selected from the group consisting of Tantalum (Ta), Tantalum Nitride (TaN), Titanium (Ti), Titanium Nitride (TiN), Silicon Nitride (SiN), and Silicon Carbide (SiC).

5. The method of claim 1 wherein substrate defines at least two spaced apart lines of metallization such that said hard mask defines unmasked areas between said two lines of metallization and said selected etched feature is a via.

6. The method of claim 1 wherein said step of providing comprises the step of providing a substrate with at least one trench defined therein, depositing a barrier liner over said at least one trench and the top surface of said dielectric, and depositing a conductive material over said substrate so as to fill said at least one trench and cover said substrate.

7. The method of claim 6 wherein said conductive material is a metal selected from the group consisting of copper and aluminum.

8. The method of claim 6 further comprising planarizing said deposited conductive material by a method selective to said barrier liner so as to remove said conductive material down to said barrier liner.

9. The method of claim 8 further comprising the step of polishing said substrate to remove said barrier liner covering said dielectric.

10. The method of claim 9 wherein said recessing step comprises the step of polishing said substrate with a material selective to said dielectric layer of said substrate such that said at least one line of metallization is recessed below the top surface of said dielectric.

11. The method of claim 1 wherein said recessing step comprises the step of polishing said substrate with a CMP (chemical-mechanical polishing) material selected to said dielectric layer of said substrate such that said at least one line of metallization is recessed below the top surface of said dielectric.

12. The method of claim 1 wherein said recessing step comprises the step of etching said conductive material selective to said dielectric material.

13. The method of claim 10 further comprising the step of depositing an ILD layer over said capping layer before depositing said layer of liner material.

14. The method of claim 10 wherein said layer of liner material is selected from the group consisting of, Tantalum (Ta), Tantalum Nitride (TaN), Titanium (Ti), Titanium Nitride (TiN), Silicon Nitride (SiN), and Silicon Carbide (SiC).

15. The method of claim 10 wherein said substrate defines at least two spaced apart lines of metallization such that said hard mask defines unmasked areas between said two lines of metallization and said selected etched feature is a via.

16. The method of claim 1 wherein said feature etched in said dielectric layer is a trench.

17. The method of claim 11 further comprising the step of depositing an ILD layer of said capping layer before depositing said layer of liner material.

18. The method of claim 11 wherein said layer of liner material is selected from the group consisting of, Tantalum (Ta), Tantalum Nitride (TaN), Titanium (Ti), Titanium Nitride (TiN), Silicon Nitride (SiN), and Silicon Carbide (SiC).

19. The method of claim 11 wherein said substrate defines at least two spaced apart lines of metallization such that said hard mask defines unmasked areas between said two lines of metallization and said selected etch feature is a via.